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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,262	11/08/2001	Daniel Gudmunson	663-169/MBE	5008

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

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DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,262	GUDMUNSON ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *12-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 18-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/02, 10/2/03* .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11 and 18-28 are drawn to data-driven synchronous parallel processing, classified in class 712, subclass 25.

II. Claim 12-17 are drawn to a way of buffering data, classified in class 712, subclass 1, with a search also in class 710, subclass 57.

2. The inventions are distinct, each from the other because of the following reasons:

3. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as standard pipeline stage buffers. See MPEP § 806.05(d).

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mark B. Eisen on July 22, 2004, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-11 and 18-28. Affirmation of this election must be made by applicant in replying to this Office action. Claims 12-17 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Claims 1-11 and 18-28 have been examined.

Drawings

7. The drawings filed on November 8, 2001 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Specification

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

9. Applicant is advised that should claim 1 be found allowable, claim 28 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-11 and 18-28 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Arvind et al., Executing a Program on the MIT Tagged-Token Dataflow Architecture, 1990, IEEE, pages 300-318, herein after "Arvind".

12. Referring to claim 1, Arvind have taught a method for data-driven synchronous parallel processing of a stream of data packets by multiple data processing units working in parallel, comprising the steps of:

a. distributing at least one instruction for data processing to one data processing unit of the multiple data processing units, before the data processing unit is available to process the instruction (page 314, Instruction tokens are sent to await instruction exewcution.);

b. storing the instruction in an execution instructions memory (Page 314, program memory);

c. sending from the one data processing unit a data request for at least one data packet corresponding to the instruction, required to execute the instruction (page 306, "read token" or "write token");

d. storing a record of the at least one data packet requested (page 306, waiting or deferred read request);

e. associating with the at least one data packet an address of the one data processing unit (pages 306, and 314-315, Section C. entitled "Multiprocessor Operation");

f. associating with the each data packet sent out a data token showing the readiness of the packet for further processing (Page 306, present, waiting, or deferred);

g. when the at least one data packet is received by the processing unit, associating the data packet with the corresponding instruction and distributing the data packet to the one data processing unit (page 306); and

h. processing the data according to the corresponding instruction (page 314, After the match occurs, the instruction is fetched and executed using the data.).

13. Referring to claim 2, Arvind has taught the method of claim 1, as described above, and wherein instructions are distributed to the multiple data processing units consecutively (Page 314, left hand column, Tokens, which are a part of the overall instruction, enter the units in sequence.).

14. Referring to claim 3, Arvind has taught the method of claim 1, as described above, and wherein instructions are distributed to the multiple data processing units concurrently (page 303, left hand column, 5th paragraph).

15. Referring to claim 4, Arvind has taught the method of claim 1, as described above, and including, after step f., the step of putting the requested data packets into an internal data buffer in a data processing unit (Page 314, WM).

16. Referring to claim 5, Arvind has taught the method of claim 1, as described above, and including, after step g., the step of erasing the record of the data request corresponding to the data packet (Page 314, When a match occurs a token is extracted.).

17. Referring to claim 6, Arvind has taught the method of claim 1, as described above, and including, during step g., the step of sending to the corresponding instruction in the execution instructions memory an indication that the at least one data packet has been received by the processing unit and is available for processing (page 314, Instruction Fetch Unit).

18. Referring to claim 7, Arvind has taught the method of claim 1, as described above, and including, during step e., the step of associating with the data packets an address of its sender and, during the step g, associating the data packet with the corresponding instruction according

to the address of the data packet sender (Page 314, Destination addresses are routed back to the top of the processing element.).

19. Referring to claim 8, Arvind has taught the method of claim 1, as described above, and including, during the step g, associating the data packet with the corresponding instruction according to the order of the data packet received (page 314, The data packets are associated as soon as they are received.).

20. Referring to claim 9, Arvind has taught the method of claim 4, as described above, and including the step of retrieving each data packet from the internal data buffer to be processed according to the corresponding instruction (Page 314, Tokens for the corresponding instruction are retrieved from the WM.).

21. Referring to claim 10, Arvind has taught the method of claim 1, as described above, and wherein an output of the processing step is sent to another data processing unit or out of the processor, or both (page 314, both).

22. Referring to claim 11, Arvind has taught the method of claim 1, as described above, and wherein processing occurs in real-time (Page 307, ID language is deterministic.).

23. Referring to claim 18, Arvind has taught an apparatus for substantially non-stalling data-driven synchronous parallel processing of data packets including a digital data processor, further comprising:

i. an interface for receiving instructions and digital data from at least one external device and sending instructions or digital data or both to at least one external device (Page 314, Output tolens to network for another PE.);

j. an instruction path contained inside the processor (Page 313-314, Instruction Fetch Unit uses an instruction path.);

k. a data path contained inside the processor; a plurality of data processing units organized for parallel processing of the data (Page 314, Paths to and from the WM.); and

l. a distributing unit organized for distributing one or more instructions at a time to the data processing units (Page 313-314, Figure 18, Instruction Fetch Unit).

24. Claim 19 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

25. Claim 20 does not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

26. Referring to claim 21, Arvind has taught the apparatus of claim 18 wherein each data processing unit comprises

a. a storage for instructions (Page 314, right hand column, 1st paragraph, program memory);

b. a storage for records of outstanding data requests (Page 314, WM);

c. a storage for receiving requested data packets (Page 314, WM); and

d. a computation module for processing the requested data packets in accordance with at least one associated instruction (Page 314, Instruction Fetch Unit, ALU).

27. Referring to claim 22, Arvind has taught the apparatus of claim 21, as described above, and comprising control logic for controlling instruction and data flows through the processor (Figure 18, "Control").

28. Referring to claim 23, Arvind has taught the apparatus of claim 18, as described above, and wherein the digital data processor comprises a general-purpose microprocessor (abstract).

29. Referring to claim 24, Arvind has taught the apparatus of claim 18, as described above, and wherein the digital data processor comprises a graphics processor (Page 301).

30. Referring to claim 25, Arvind has taught the apparatus of claim 18, as described above, and wherein the digital data processor comprises a digital signal processor (abstract, page 301).

31. Referring to claim 26, Arvind has taught the apparatus of claim 21, as described above, and wherein the computational module operates using vector values (Page 301).

32. Referring to claim 27, Arvind has taught the apparatus of claim 21, as described above, and wherein the computational module operates using scalar values (Page 301, Where the vector size is 1.).

33. Claim 28 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

Conclusion

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER